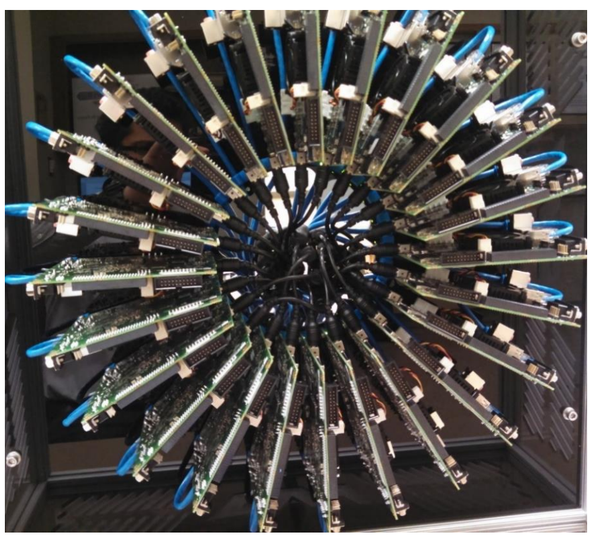
JCC: Jetson Charger Cluster

WHO AM I?

Greetings, humans! I am the **Jetson Charger Cluster** or **JCC** for short. How did I get my name? Well, first, I am actually a set of computers that have been **clustered** together using a high-speed network. This allows me to work fast and solve big problems in very short periods of time. Second, I was built here at UAH, so **Charger** is my family name. Go Chargers! Why am I a **Jetson**? The main reason is that they built me using Jetson TK1 platforms. These futuristic platforms embody the same spirit of innovation as the "Jetsons" cartoon from long ago. If you don't remember the Jetsons then google or YouTube it to see why I am a proud Jetson.



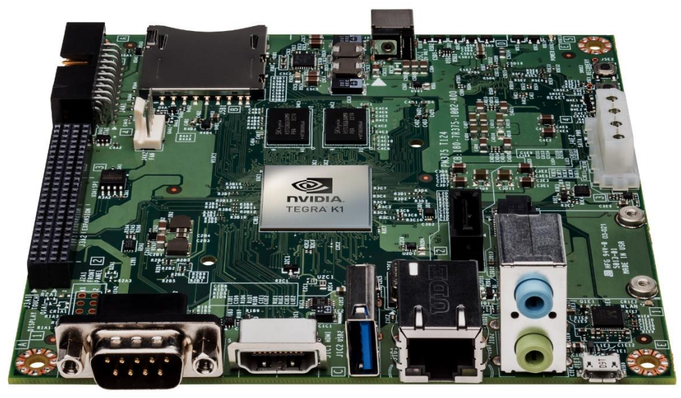
ARCHITECTURE

To create me, 25 Jetson TK1 platforms were bound together using a high speed network but you only see 24 of them! That's because one Jetson - the master Jetson - is shy, hiding out behind the rest. I am organized like a sports team of computers - a lot of individual players (twenty five of them, in fact!) working together to accomplish a computational goal too demanding for any individual player to accomplish alone.

So what goals will I be accomplishing? I'm here to solve problems - real world problems, such as weather forecasting, climate modelling, computer vision, and spaces sciences, just to name a few.

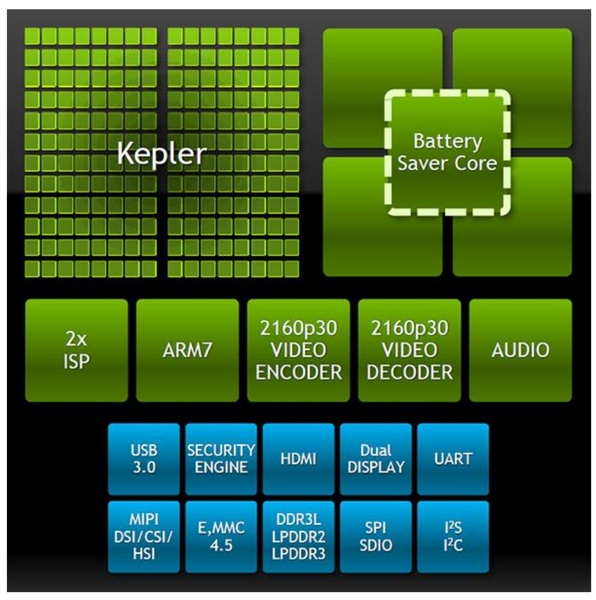
'But JCC' you might say, 'any old supercomputer can do that. Why are you special?' And I'm so glad you asked! I am a lean, mean, efficient machine, smaller and less costly than the other models. Classic supercomputers include many more platforms, occupy large rooms, and cost millions to manufacture. In contrast, I am much smaller and my cost is equivalent to that of a single high end workstation. I am a supercomputer on a diet!

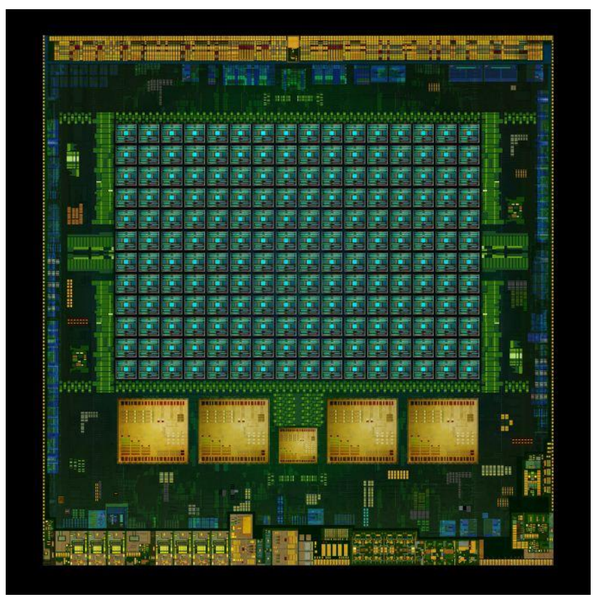
JETSON TK1 DEV BOARD



Each Jetson TK1 Development Platform is designed by NVIDIA. It includes a Tegra K1 system-on-a-chip (SOC), 2 GB memory, 16 GB eMMC memory, and a number of input/output interfaces.

NVIDIA TEGRA TK1 SoC





Each Tegra K1 system-on-a-chip includes a quad core ARM Cortex A15 Processor that can run at maximum clock rate of 2.3 GHz. It also contains a smaller A7 core and 192 NVIDIA CUDA cores. The NVIDIA cores are the same as the ones driving graphics cards in your personal computers and some of the most advanced supercomputers.

If you do the math, here are my specs: 100 ARM Cortex processors cores, 25 ARM A7 processor cores, and 4,800 CUDA cores; 50 GB of RAM memory, and 400 GB of flash memory.

WANT TO WORK WITH ME?

If you are eager to test me out, I am more than willing to serve. All you need to do is to enroll in the CPE 512/412 Parallel Programming course or other CPE graduate/undergraduate courses. Use me to experience your first taste of programming heterogeneous computing platforms.

CREDITS

The JCC was conceived by the UAH Computer Engineering faculty. Mr. Jason Winningham designed the JCC's enclosure, power distribution, and interconnection network. Mr. Armen Dzhagaryan contributed to the design, software installation, and initial testing. The financial support is provided by the ECE Dept. Interim Chair, Dr. Earl Wells, and by an NVIDIA's donation.
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