CPE 323: MSP430 Clocks

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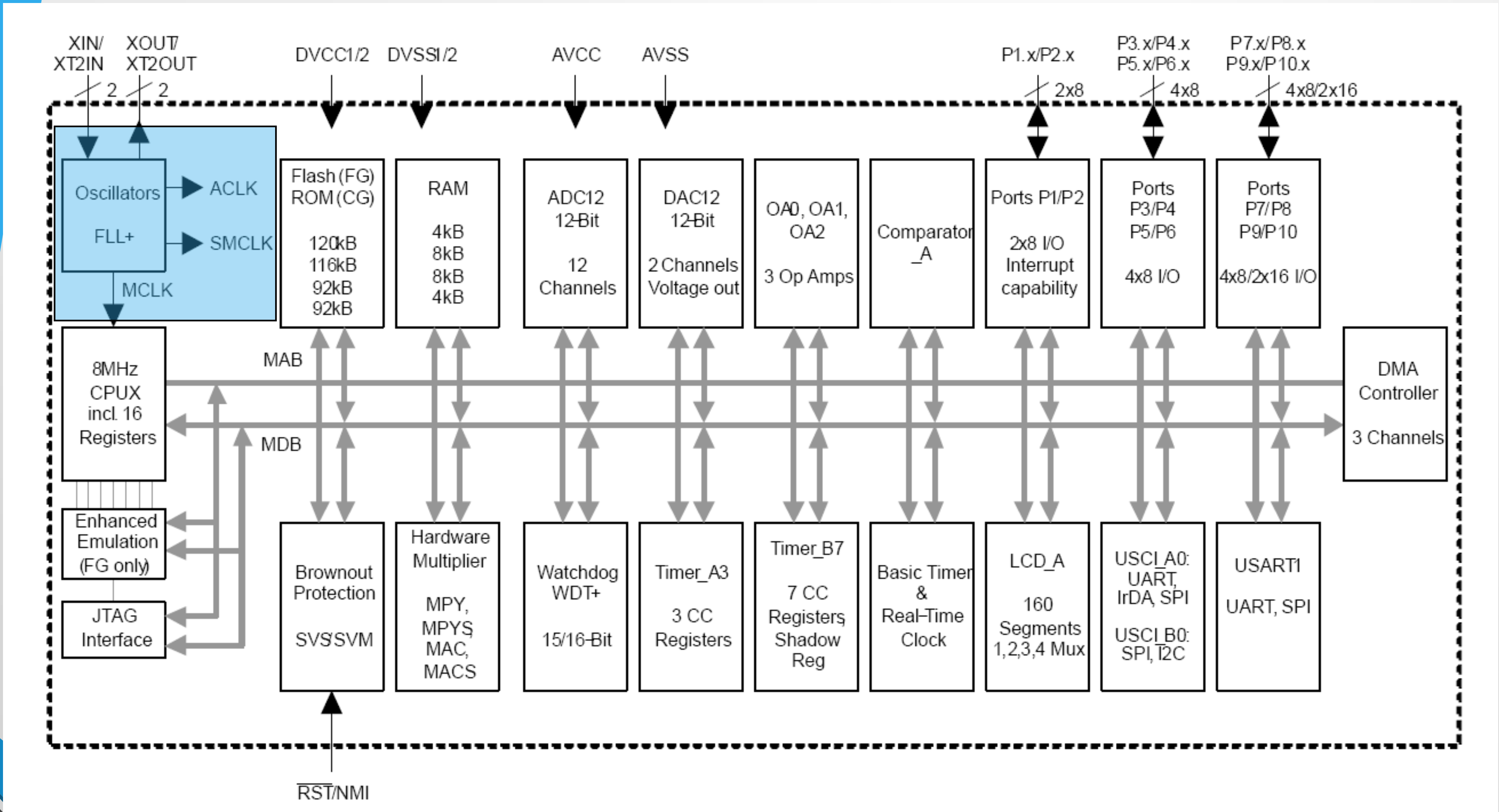
Outline

- Clocks
- MSP430 Clock System
- FLL+ Module
- FLL+ Registers
- Demos

MSP430xG461x Microcontroller



Clocks

- Clock: a square wave whose edges trigger hardware state changes
- Traditional clock: a crystal with frequency of a few MHz is connected to two μC pins; internally the clock may be divided by 2 or 4
- Typical application cycle in embedded systems
  - μC stays in a low-power mode until
  - An event wakes up μC to handle it
- Often need multiple clocks (fast for CPU, slow for peripherals)
- Power consumption: P ~ CV^2f

Clock Types

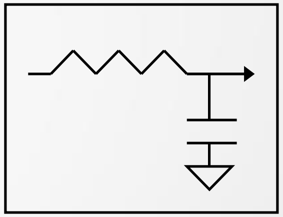
- Crystal clocks
  - Accurate (the frequency is typically within 11 part in 100,000), stable (do not change with time or temperature)
  - High-frequency (a few MHz) or low-frequency (32,768 Hz) for a real-time clock
  - Expensive, delicate, draw a relatively large current, require additional components (capacitors), take long time to start up and stabilize
- Resistor and capacitor (RC) clocks
  - Cheap, quick to start
  - Poor accuracy and stability
  - Can be external or integrated into a chip

MSP430 Clock System

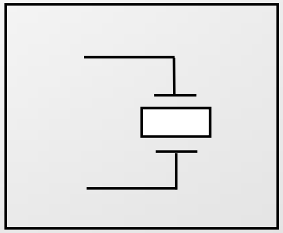
- Flexible to address conflicting demands for high-performance, low-power, and a precise frequency
- 3 internal clocks from 4 possible sources: MCLK, SMCLK, ACLK
- Master clock, MCLK: used by the CPU and a few peripherals (e.g., ADC12, DMA, ...)
- Subsystem master clock, SMCLK: distributed to peripherals
- Auxiliary clock, ACLK: distributed to peripherals
- Typical configuration: MCLK and SMCLK are in the megahertz range, ACLK is 32 KHz

MSP430 Clock System

- Digitally controlled Oscillator, DCO: available in all devices; highly-controllable oscillator
  - Generated on-chip RC-type frequency controlled by SW + HW



- Low- or high-frequency crystal oscillator, LFXT1
  - LF: 32768Hz
  - XT: 450kHz 8MHz



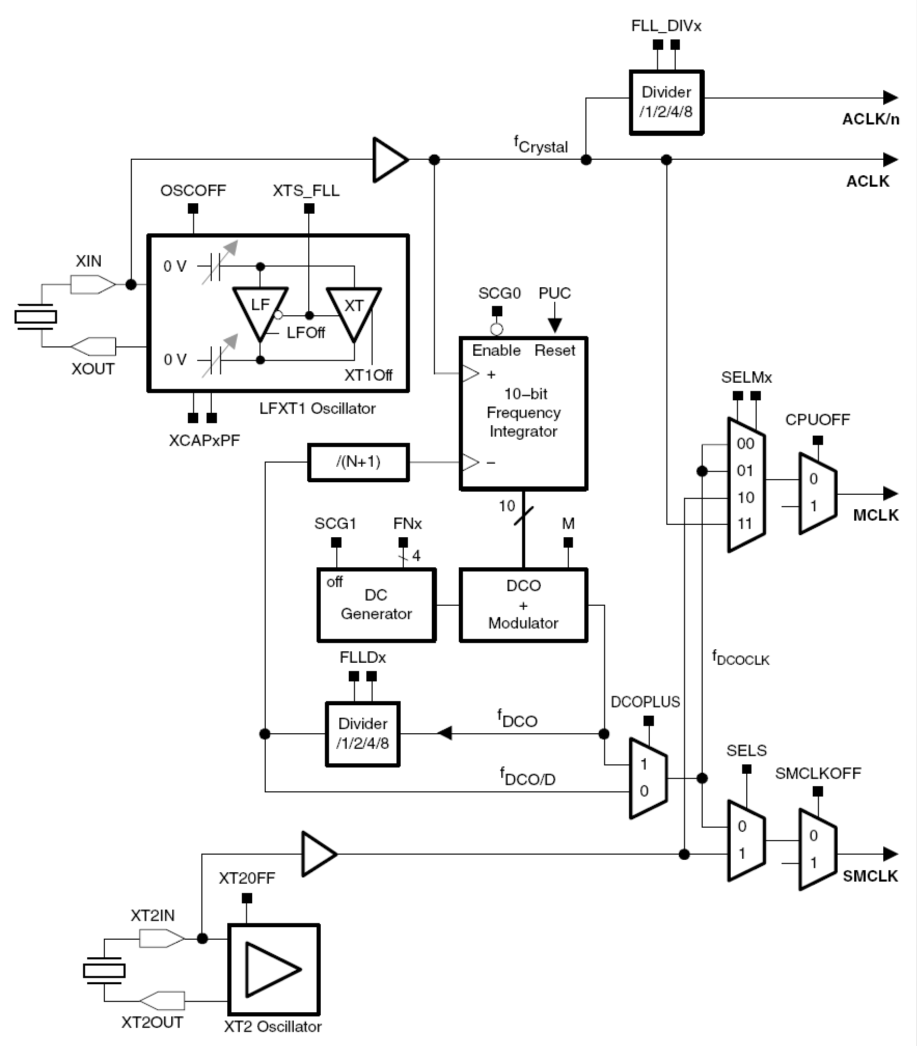
- High-frequency crystal oscillator, XT2
- Internal very low-power, low-frequency oscillator, VLO: available in more recent MSP430F2xx devices; provides an alternative to LFXT1 when accuracy is not needed

FLL+ Clock Module (MSP430x4xx)

- FLL+ clock module: frequency-locked loop clock module
- Characteristics
  - Low system cost
  - Ultra-low power consumption
  - Can operate with no external components
  - Supports one or two external crystals or resonators (LFXT1 and XT2)
  - Internal digitally-controlled oscillator with stabilization to a multiple of the LFXT1 watch crystal frequency
  - Full software control over 4 output clocks: ACLK, ACLK/n, MCLK, and SMCLK

FLL+ Block Diagram

- LFXT1CLK: Low-frequency/high-frequency oscillator that can be used
  - either with low-frequency 32768-Hz watch crystals, or
  - standard crystals or resonators in the 450-kHz to 8-MHz range
- XT2CLK: Optional high-frequency oscillator that can be used with standard crystals, resonators, or external clock sources in the 450-kHz to 8-MHz range
- DCOCLK: Internal digitally controlled oscillator (DCO) with RC-type characteristics, stabilized by the FLL.



FLL+ Clocks

- ACLK: Auxiliary clock
  - The ACLK is the LFXT1CLK clock source. ACLK is software selectable for individual peripheral modules
- ACLK/n: Buffered output of the ACLK
  - The ACLK/n is ACLK divided by 1,2,4 or 8 and only used externally
- MCLK: Master clock used by the CPU and system
  - Software selectable as LFXT1CLK, XT2CLK (if available), or DCOCLK
  - MCLK can be divided by 1, 2, 4, or 8 within the FLL block
- SMCLK: Sub-main clock, used by peripheral modules
  - Software selectable as XT2CLK (if available), or DCOCLK

FLL+ Operation

- After a PUC, MCLK and SMCLK are sourced from DCOCLK at 32 times the ACLK frequency
    - When a 32,768-Hz crystal is used for ACLK, MCLK and SMCLK will stabilize to 1.048576 MHz
- Status register control bits SCG0, SCG1, OSCOFF, and CPUOFF configure the MSP430 operating modes and enable or disable components of the FLL+ clock module
- SCFQCTL, SCFI0, SCFI1, FLL_CTL0, and FLL_CTL1 registers configure the FLL+ clock module
    - FLL+ can be configured or reconfigured by software at any time during program execution.
- Example, MCLK = 64 × ACLK = 2097152

```
BIC #GIE,SR ; Disable interrupts

MOV.B #(64-1),&SCFQTL ; MCLK = 64 * ACLK, DCOPLUS=0

MOV.B #FN_2,&SCFIO ; Select DCO range

BIS #GIE,SR ; Enable interrupts
```

LFXT1

- Low-frequency (LF) mode (XTS_FLL=0) with 32,768 Hz watch crystal connected to XIN and XOUT
- High-frequency (HF) mode (XTS_FLL=1) with high-frequency crystals or resonators connected to XIN and XOUT (~450 KHz to 8 MHz)
- XCPxPF bits configure the internally provided load capacitance for the LFXT1 crystal (1, 6, 8, or 10 pF)
- OSCOFF bit can be set to disable LFXT1

XT2

- XT2 sources XT2CLK and its characteristics are identical to LFXT1 in HF mode, except it does not have internal load capacitors (must be provided externally)
- XT2OFF bit disables the XT2 oscillator if XT2CLK is not used for MCLK and SMCLK

DCO

- Integrated ring oscillator with RC-type characteristics
- DCO frequency is stabilized by the FLL to a multiple of ACLK as defined by N (the lowest 7 bits of the SCFQCTL register)
- DCOPLUS bit sets the f_{DCOCLK} to f_{DCO} or $f_{DCO/D}$ (divider)
  - FLLDx bits define the divider D to 1, 2, 4 or 8
  - By default DCOPLUS=0 and D=2 (providing $f_{DCOCLK}= f_{DCO/2}$)
- DCOPLUS = 0: $f_{DCOCLK} = (N + 1) \times f_{ACLK}$
- DCOPLUS = 1: $f_{DCOCLK} = D \times (N + 1) \times f_{ACLK}$

Frequency Locked Loop

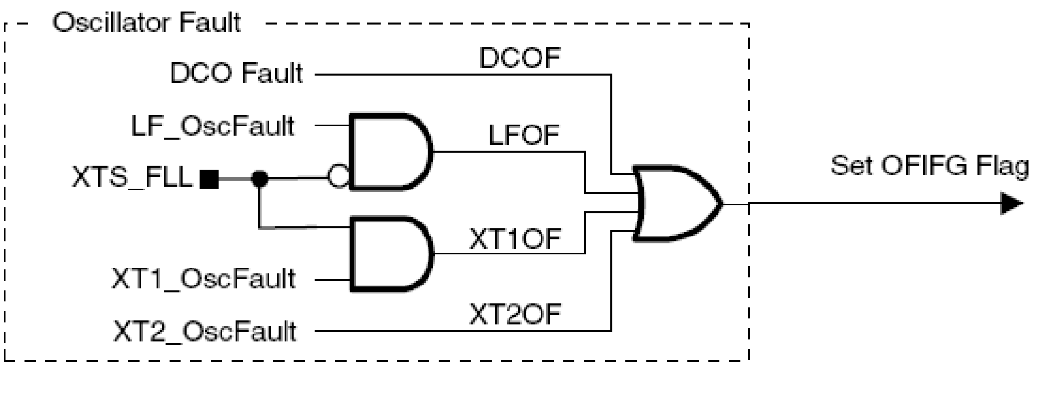
- FLL continuously counts up or down a 10-bit frequency integrator
- The output of the frequency integrator that drives the DCO can be read in SCFI1 and SCFI0. The count is adjusted +1 or −1 with each ACLK crystal period.
- Five of the integrator bits, SCFI1 bits 7-3, set the DCO frequency tap
  - Twenty-nine taps are implemented for the DCO (28, 29, 30, and 31 are equivalent), and each is approximately 10% higher than the previous
  - The modulator mixes two adjacent DCO frequencies to produce fractional taps
- SCFI1 bits 2-0 and SCFI0 bits 1-0 are used for the modulator
- The DCO starts at the lowest tap after a PUC or when SCFI0 and SCFI1 are cleared
  - Time must be allowed for the DCO to settle on the proper tap for normal operation. 32 ACLK cycles are required between taps requiring a worst case of 28 x 32 ACLK cycles for the DCO to settle

DCO Modulator

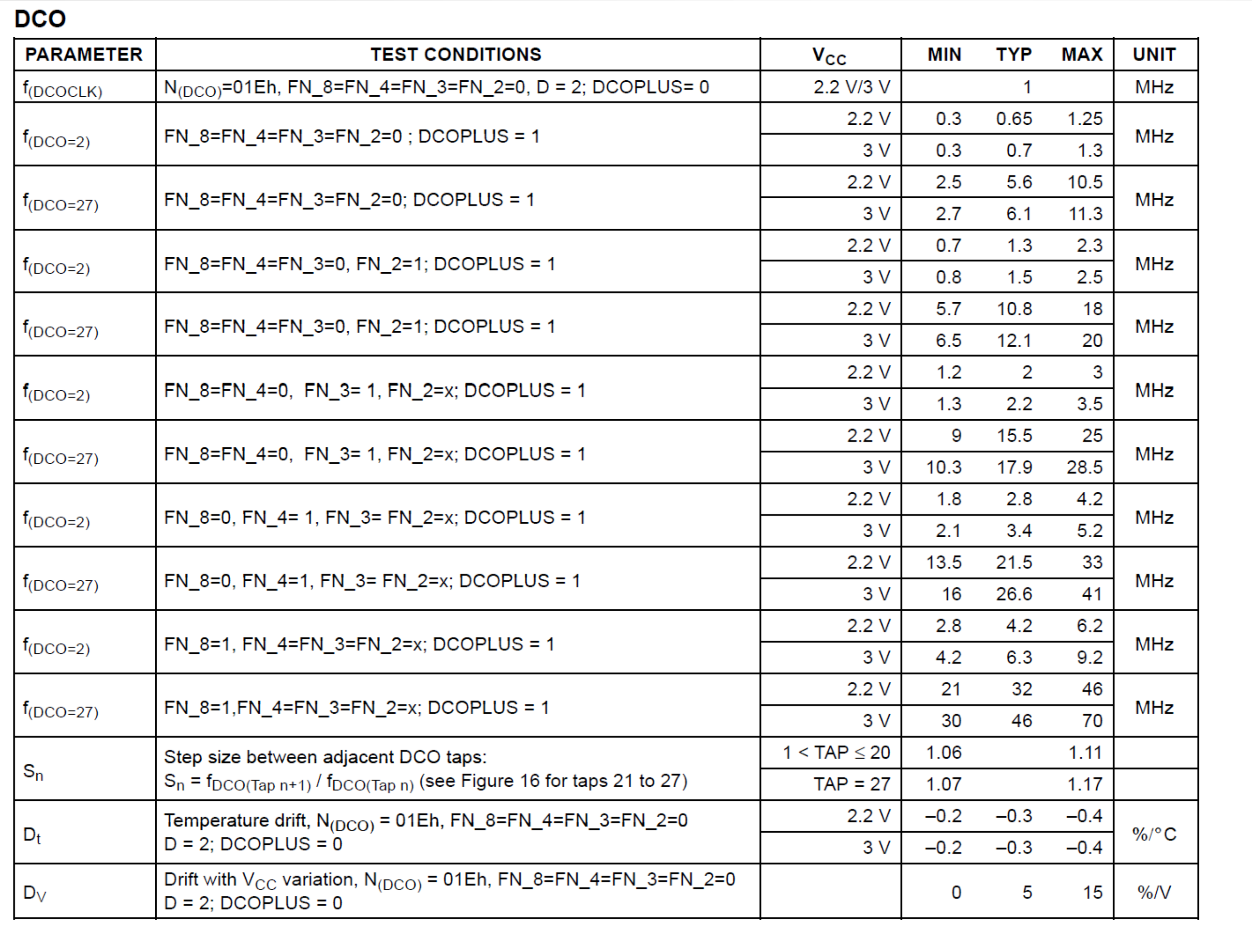
- Mixes two adjacent DCO frequencies to produce an intermediate effective frequency and spread the clock energy, reducing electromagnetic interference (EMI)
- Mixes the two adjacent frequencies across 32 DCOCLK clock cycles
- The error of the effective frequency is zero every 32 DCOCLK cycles and does not accumulate
    - Modulator settings and DCO control are automatically controlled by the FLL hardware

Fail Safe Operation

- ncorporates an oscillator-fault fail-safe feature
  - Detects an oscillator fault for LFXT1, DCO and XT2
- Available fault conditions are:
  - Low-frequency oscillator fault (LFOF) for LFXT1 in LF mode
  - High-frequency oscillator fault (XT1OF) for LFXT1 in HF mode
  - High-frequency oscillator fault (XT2OF) for XT2
  - DCO fault flag (DCOF) for the DCO



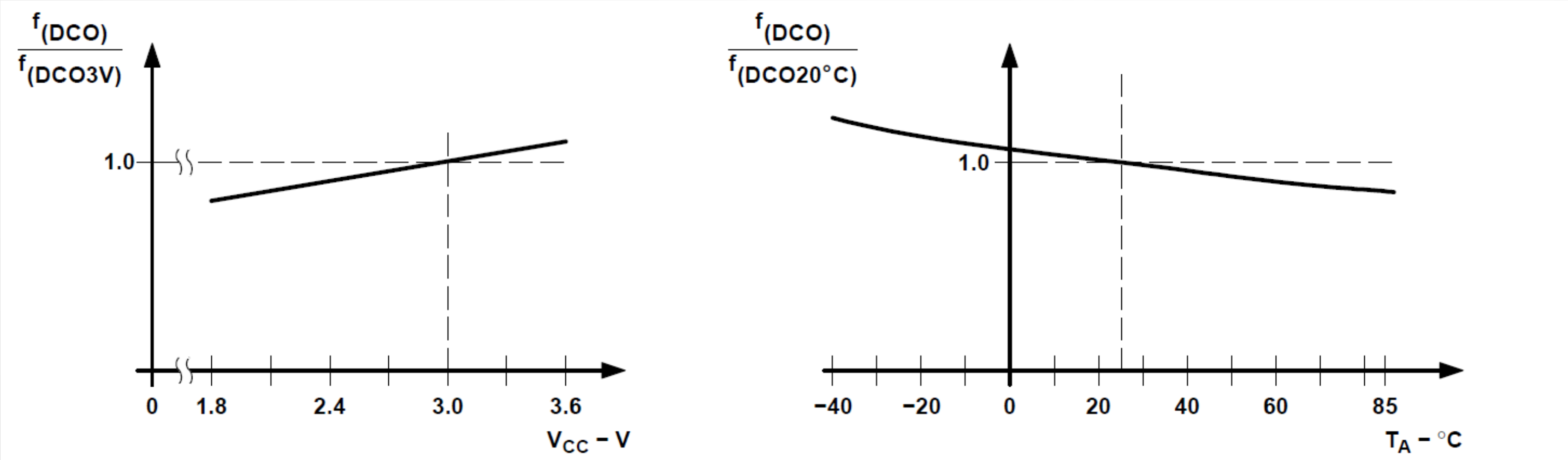
DCO Frequency Range



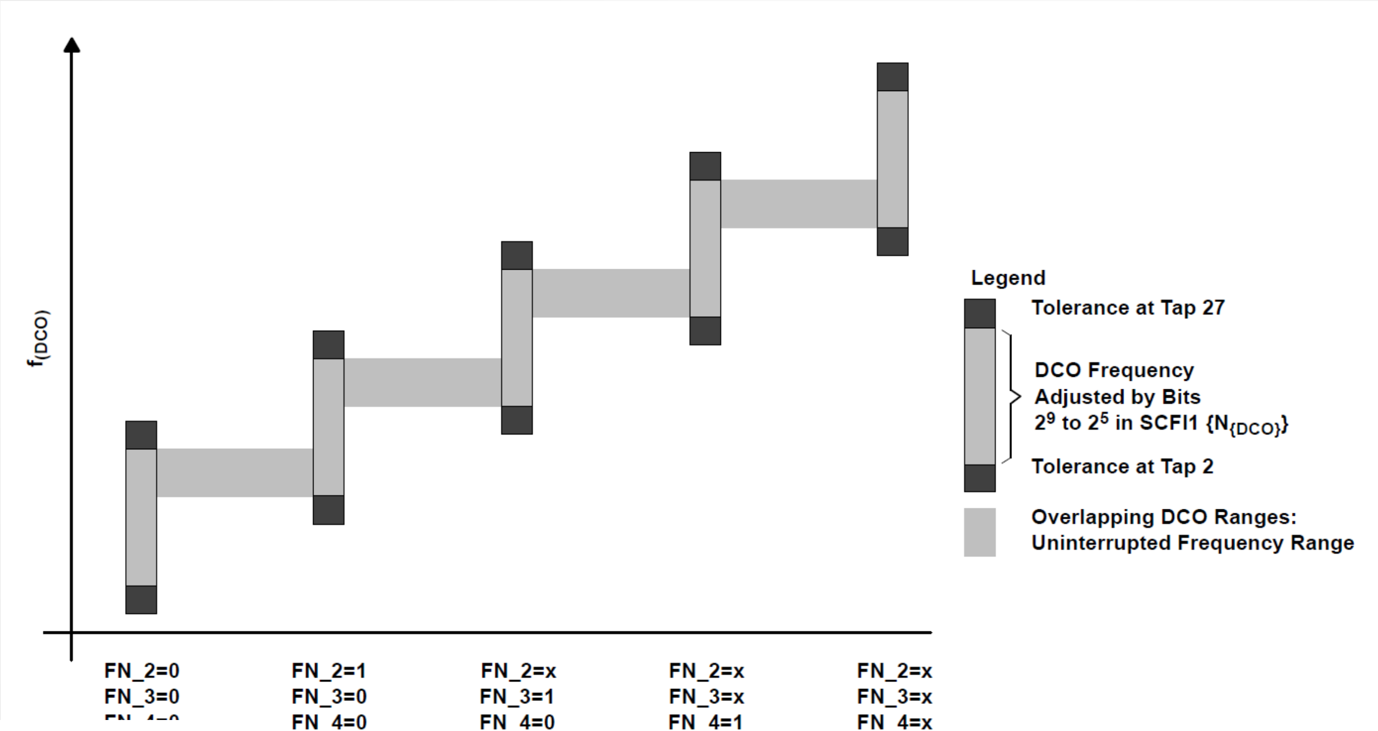
DCO

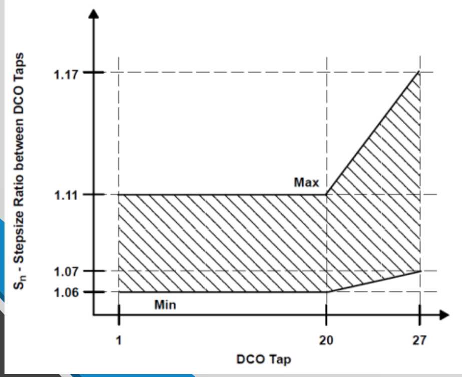
PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01Eh, FN_8=FN_4=FN_3=FN_2=0, D = 2; DCOPLUS= 0	2.2 V/3 V		1		MHz
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=FN_2=0 ; DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO=27)}$	FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO=27)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO=2)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO=27)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO=2)}$	FN_8=0, FN_4= 1, FN_3= FN_2=x; DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO=27)}$	FN_8=0, FN_4=1, FN_3= FN_2=x; DCOPLUS = 1	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO=2)}$	FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO=27)}$	FN_8=1,FN_4=FN_3=FN_2=x; DCOPLUS = 1	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$ (see Figure 16 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01Eh, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0		0	5	15	%/V

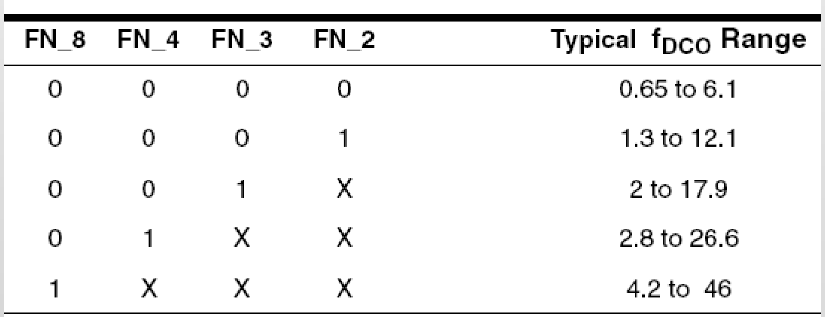
DCO Frequency as f(VCC, TA)



DCO Ranges
Controlled by FN bits

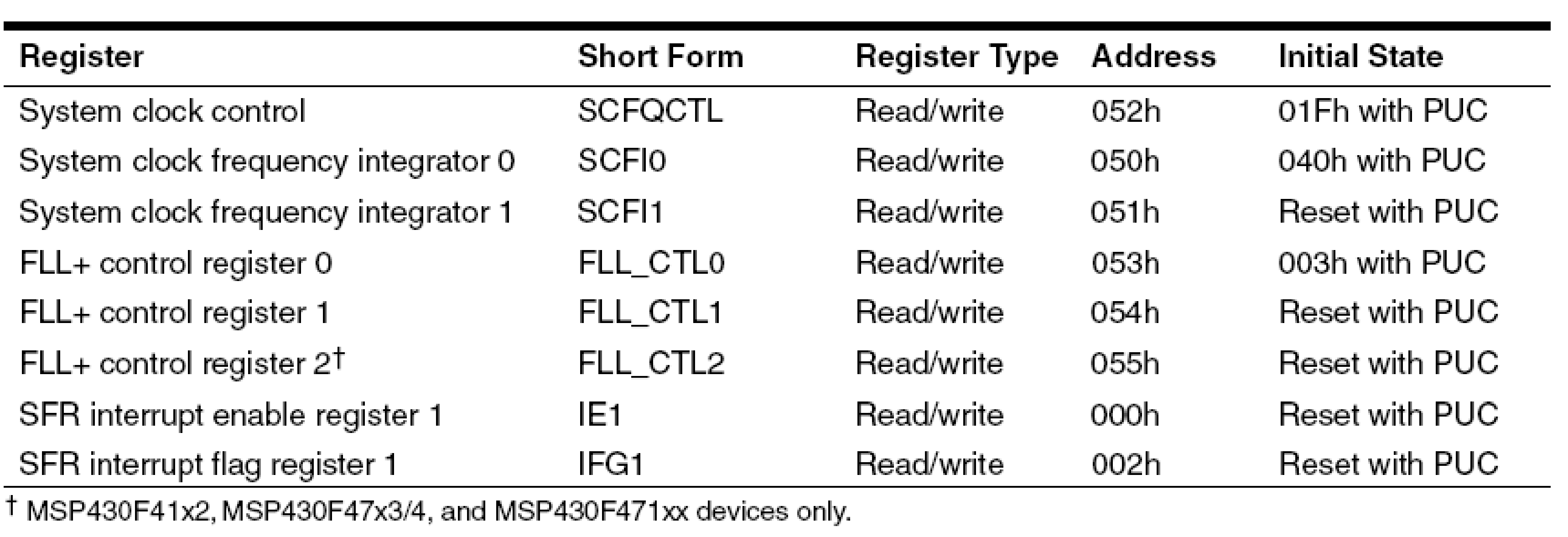






FN_8	FN_4	FN_3	FN_2	Typical f_{DCO} Range
0	0	0	0	0.65 to 6.1
0	0	0	1	1.3 to 12.1
0	0	1	X	2 to 17.9
0	1	X	X	2.8 to 26.6
1	X	X	X	4.2 to 46

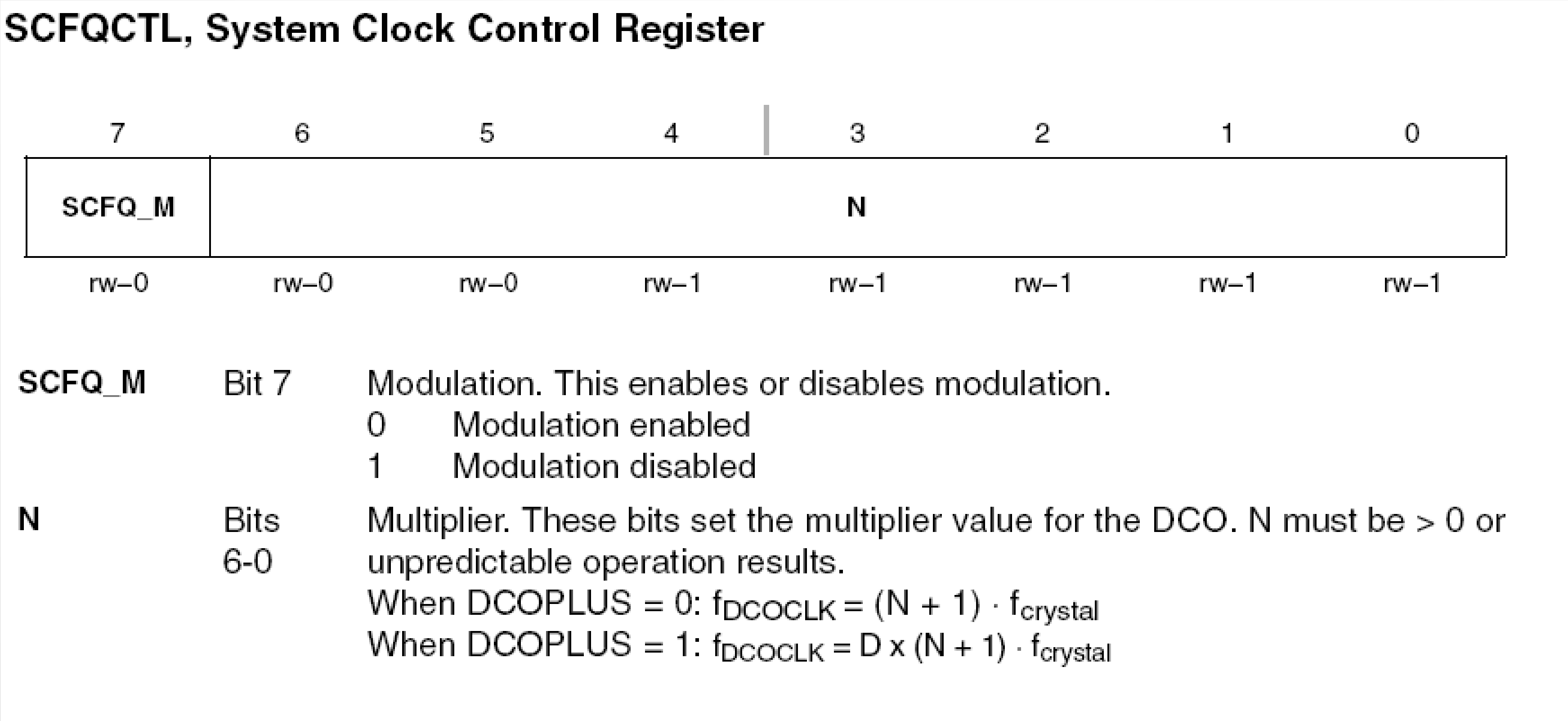
FLL+ Registers



Register	Short Form	Register Type	Address	Initial State
System clock control	SCFQCTL	Read/write	052h	01Fh with PUC
System clock frequency integrator 0	SCFI0	Read/write	050h	040h with PUC
System clock frequency integrator 1	SCFI1	Read/write	051h	Reset with PUC
FLL+ control register 0	FLL_CTL0	Read/write	053h	003h with PUC
FLL+ control register 1	FLL_CTL1	Read/write	054h	Reset with PUC
FLL+ control register 2[†]	FLL_CTL2	Read/write	055h	Reset with PUC
SFR interrupt enable register 1	IE1	Read/write	000h	Reset with PUC
SFR interrupt flag register 1	IFG1	Read/write	002h	Reset with PUC

[†] MSP430F41x2, MSP430F47x3/4, and MSP430F471xx devices only.

FLL+: SCFQCTL

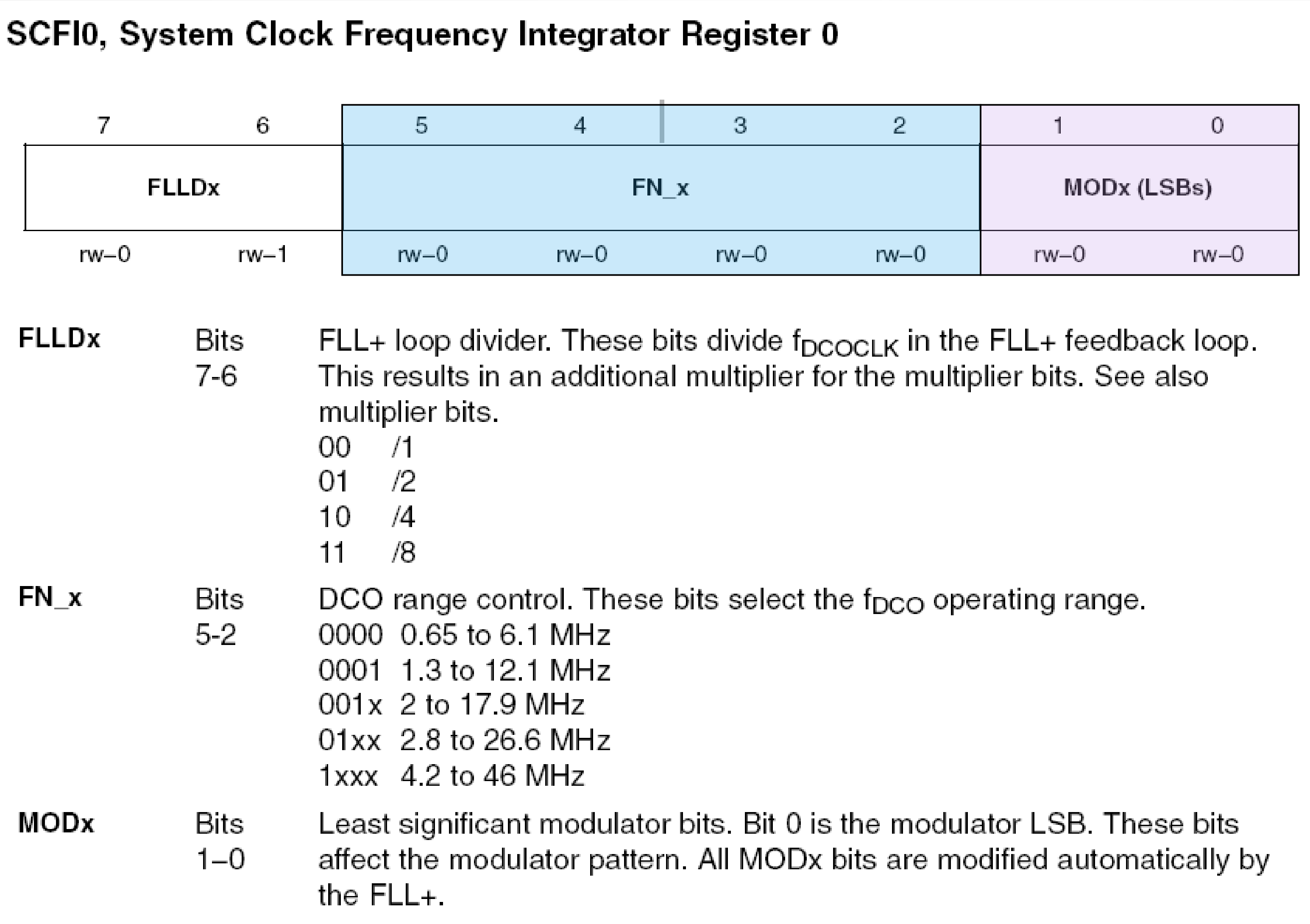


SCFQCTL, System Clock Control Register

7	6	5	4	3	2	1	0
SCFQ_M	N						
rw–0	rw–0	rw–0	rw–1	rw–1	rw–1	rw–1	rw–1

SCFQ_M	Bit 7	Modulation. This enables or disables modulation. 0 Modulation enabled 1 Modulation disabled
N	Bits 6-0	Multiplier. These bits set the multiplier value for the DCO. N must be > 0 or unpredictable operation results. When DCOPLUS = 0: $f_{DCOCLK} = (N + 1) \cdot f_{crystal}$ When DCOPLUS = 1: $f_{DCOCLK} = D \times (N + 1) \cdot f_{crystal}$

SCFI0



SCFI0, System Clock Frequency Integrator Register 0

7	6	5	4	3	2	1	0
FLLDx		FN_x				MODx (LSBs)	
rw–0	rw–1	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

FLLDx Bits 7-6 FLL+ loop divider. These bits divide f_{DCOCLK} in the FLL+ feedback loop. This results in an additional multiplier for the multiplier bits. See also multiplier bits.

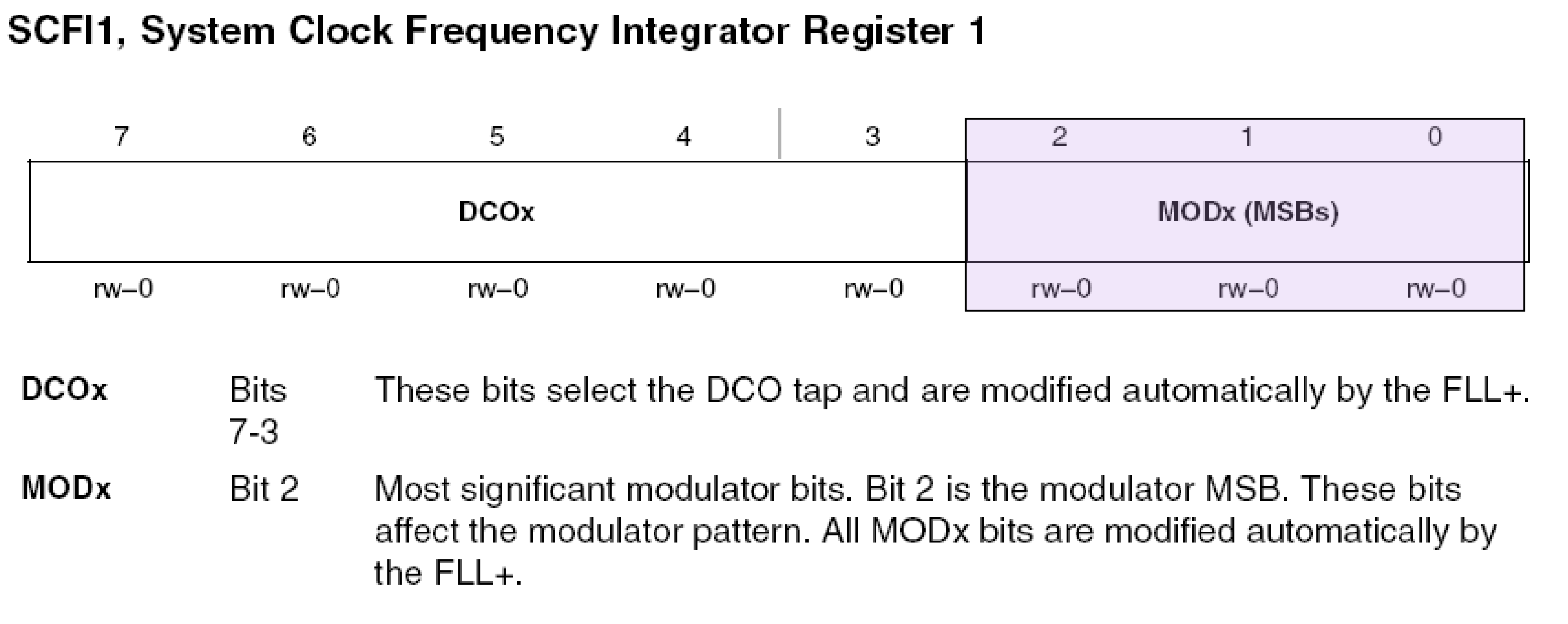
00	/1
01	/2
10	/4
11	/8

FN_x Bits 5-2 DCO range control. These bits select the f_{DCO} operating range.

0000	0.65 to 6.1 MHz
0001	1.3 to 12.1 MHz
001x	2 to 17.9 MHz
01xx	2.8 to 26.6 MHz
1xxx	4.2 to 46 MHz

MODx Bits 1–0 Least significant modulator bits. Bit 0 is the modulator LSB. These bits affect the modulator pattern. All MODx bits are modified automatically by the FLL+.

SCFI1

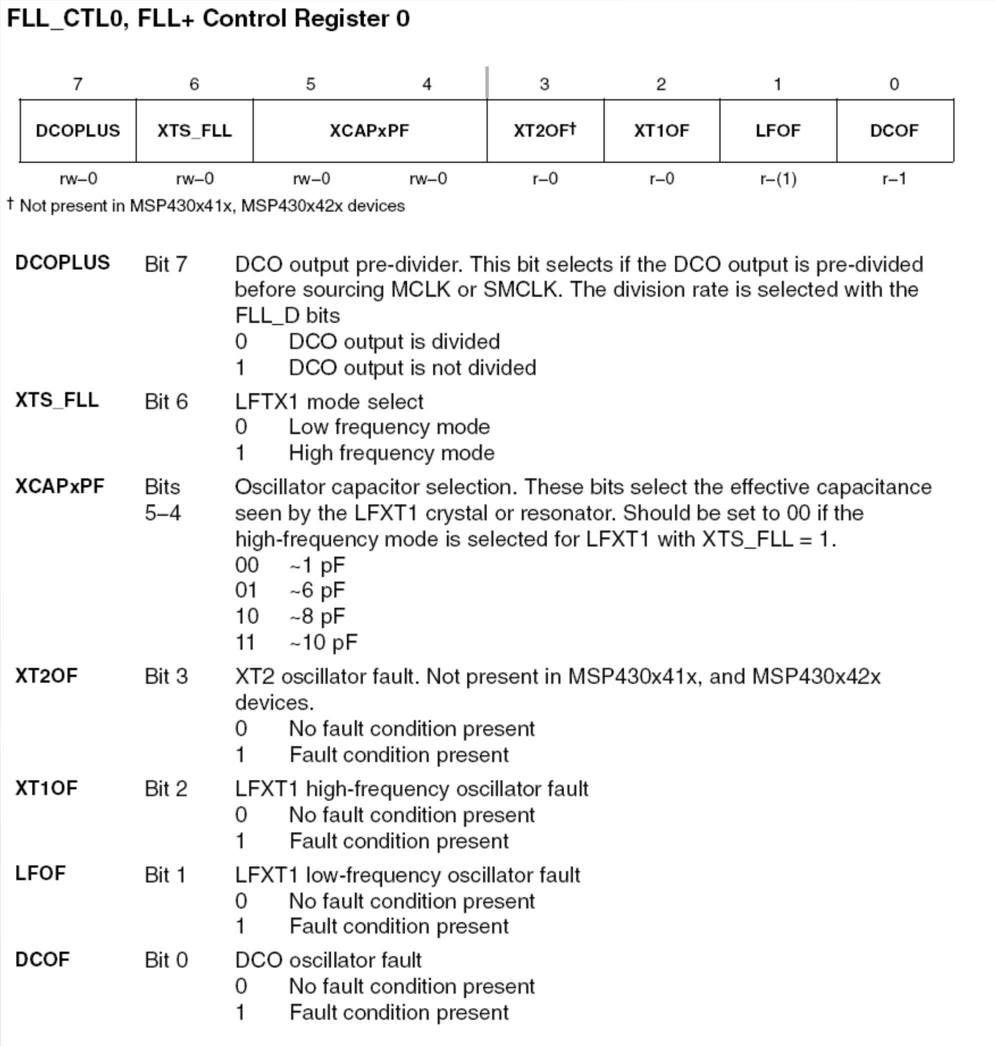


SCFI1, System Clock Frequency Integrator Register 1

7	6	5	4	3	2	1	0
DCOx					MODx (MSBs)		
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

DCOx	Bits 7-3	These bits select the DCO tap and are modified automatically by the FLL+.
MODx	Bit 2	Most significant modulator bits. Bit 2 is the modulator MSB. These bits affect the modulator pattern. All MODx bits are modified automatically by the FLL+.

FLL_CTL0



FLL_CTL0, FLL+ Control Register 0

7	6	5	4	3	2	1	0
DCOPLUS	XTS_FLL	XCAPxPF		XT2OF†	XT1OF	LFOF	DCOF
rw–0	rw–0	rw–0	rw–0	r–0	r–0	r–(1)	r–1

† Not present in MSP430x41x, MSP430x42x devices

DCOPLUS Bit 7 DCO output pre-divider. This bit selects if the DCO output is pre-divided before sourcing MCLK or SMCLK. The division rate is selected with the FLL_D bits
0 DCO output is divided
1 DCO output is not divided

XTS_FLL Bit 6 LFTX1 mode select
0 Low frequency mode
1 High frequency mode

XCAPxPF Bits 5–4 Oscillator capacitor selection. These bits select the effective capacitance seen by the LFXT1 crystal or resonator. Should be set to 00 if the high-frequency mode is selected for LFXT1 with XTS_FLL = 1.
00 ~1 pF
01 ~6 pF
10 ~8 pF
11 ~10 pF

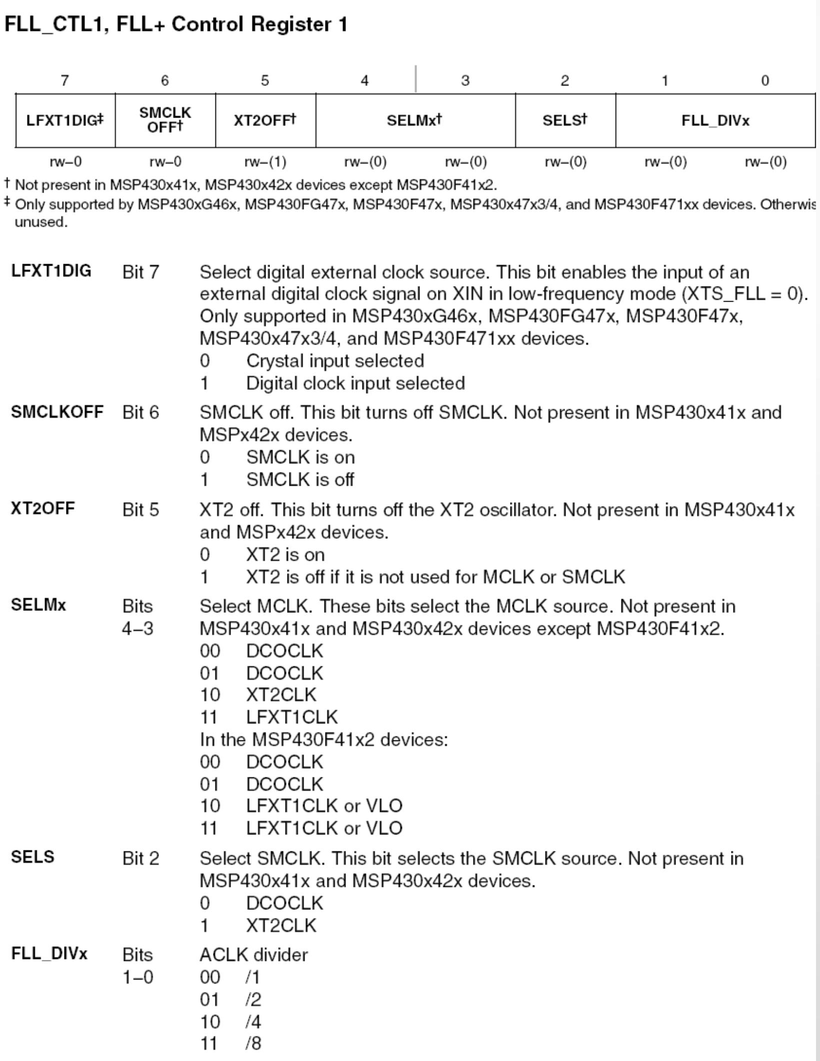
XT2OF Bit 3 XT2 oscillator fault. Not present in MSP430x41x, and MSP430x42x devices.
0 No fault condition present
1 Fault condition present

XT1OF Bit 2 LFXT1 high-frequency oscillator fault
0 No fault condition present
1 Fault condition present

LFOF Bit 1 LFXT1 low-frequency oscillator fault
0 No fault condition present
1 Fault condition present

DCOF Bit 0 DCO oscillator fault
0 No fault condition present
1 Fault condition present

FLL_CTL1



FLL_CTL1, FLL+ Control Register 1

7	6	5	4	3	2	1	0
LFXT1DIG‡	SMCLK OFF†	XT2OFF†	SELMx†		SELS†	FLL_DIVx	
rw–0	rw–0	rw–(1)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

† Not present in MSP430x41x, MSP430x42x devices except MSP430F41x2.

‡ Only supported by MSP430xG46x, MSP430FG47x, MSP430F47x, MSP430x47x3/4, and MSP430F471xx devices. Otherwis unused.

LFXT1DIG Bit 7 Select digital external clock source. This bit enables the input of an external digital clock signal on XIN in low-frequency mode (XTS_FLL = 0). Only supported in MSP430xG46x, MSP430FG47x, MSP430F47x, MSP430x47x3/4, and MSP430F471xx devices.

0	Crystal input selected
1	Digital clock input selected

SMCLKOFF Bit 6 SMCLK off. This bit turns off SMCLK. Not present in MSP430x41x and MSPx42x devices.

0	SMCLK is on
1	SMCLK is off

XT2OFF Bit 5 XT2 off. This bit turns off the XT2 oscillator. Not present in MSP430x41x and MSPx42x devices.

0	XT2 is on
1	XT2 is off if it is not used for MCLK or SMCLK

SELMx Bits 4–3 Select MCLK. These bits select the MCLK source. Not present in MSP430x41x and MSP430x42x devices except MSP430F41x2.

00	DCOCLK
01	DCOCLK
10	XT2CLK
11	LFXT1CLK

In the MSP430F41x2 devices:

00	DCOCLK
01	DCOCLK
10	LFXT1CLK or VLO
11	LFXT1CLK or VLO

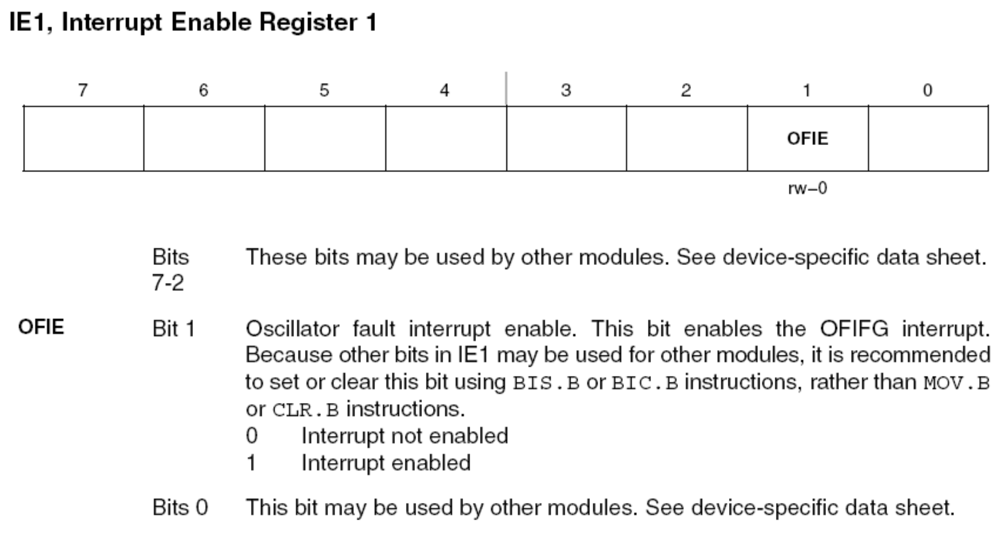
SELS Bit 2 Select SMCLK. This bit selects the SMCLK source. Not present in MSP430x41x and MSP430x42x devices.

0	DCOCLK
1	XT2CLK

FLL_DIVx Bits 1–0 ACLK divider

00	/1
01	/2
10	/4
11	/8

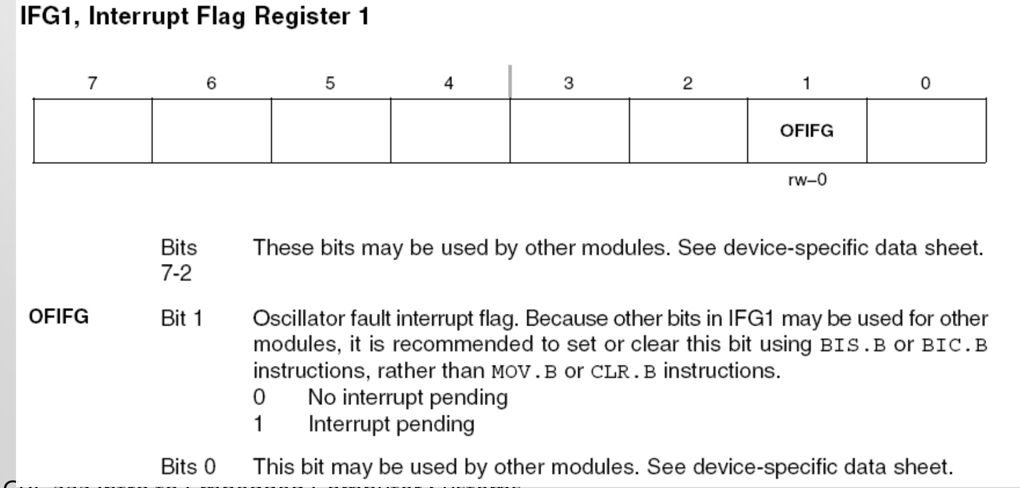
IFG1, IE1



IE1, Interrupt Enable Register 1

7	6	5	4	3	2	1	0
						OFIE	
						rw–0	

	Bits 7-2	These bits may be used by other modules. See device-specific data sheet.
OFIE	Bit 1	Oscillator fault interrupt enable. This bit enables the OFIFG interrupt. Because other bits in IE1 may be used for other modules, it is recommended to set or clear this bit using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions. 0 Interrupt not enabled 1 Interrupt enabled
	Bits 0	This bit may be used by other modules. See device-specific data sheet.



IFG1, Interrupt Flag Register 1

7	6	5	4	3	2	1	0
						OFIFG	
						rw–0	

	Bits 7-2	These bits may be used by other modules. See device-specific data sheet.
OFIFG	Bit 1	Oscillator fault interrupt flag. Because other bits in IFG1 may be used for other modules, it is recommended to set or clear this bit using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions. 0 No interrupt pending 1 Interrupt pending
	Bits 0	This bit may be used by other modules. See device-specific data sheet.

Demo #1 (DCO @ 2.45 MHz)

```
//*******************************************************************************
//  MSP430xG46x Demo - FLL+, Runs Internal DCO at 2.45MHz
//  Description: This program demonstrates setting the internal DCO to run at
//  2.45MHz with auto-calibration by the FLL+ circuitry.
//  ACLK = LFXT1 = 32768Hz, MCLK = SMCLK = DCO = (74+1) x ACLK = 2457600Hz
//                 MSP430xG461x
//             -----------------
//         /|\|              XIN|-
//          | |                 | 32kHz
//          --|RST          XOUT|-
//            |                 |
//            |             P1.1|--> MCLK = 2.45MHz
//            |                 |
//            |             P1.5|--> ACLK = 32kHz
//            |                 |
//******************************************************************************
#include  <msp430xG46x.h>

void main(void)
{
  WDTCTL = WDTPW + WDTHOLD;                 // Stop watchdog timer
  FLL_CTL0 |= XCAP18PF;                     // Set load capacitance for xtal
  SCFI0 |= FN_2;                            // x2 DCO, 4MHz nominal DCO
  SCFQCTL = 74;                             // (74+1) x 32768 = 2.45Mhz

  P1DIR = 0x22;                             // P1.1 & P1.5 to output direction
  P1SEL = 0x22;                             // P1.1 & P1.5 to output MCLK & ACLK
  while(1);                                 // Loop in place
}
```

Demo #2 (DCO @ 8 MHz)

```
//******************************************************************************
//  MSP430xG46x Demo - FLL+, Runs Internal DCO at 8MHz
//  Description: This program demonstrates setting the internal DCO to run at
//  8MHz with auto-calibration by the FLL+.
//  ACLK = LFXT1 = 32768Hz, MCLK = SMCLK = DCO = (121+1) x 2 x ACLK = 7995392Hz
//                 MSP430xG461x
//             -----------------
//         /|\|              XIN|-
//          | |                 | 32kHz
//          --|RST          XOUT|-
//            |                 |
//            |             P1.1|--> MCLK = 8MHz
//            |                 |
//            |             P1.5|--> ACLK = 32kHz
//
//******************************************************************************
#include  <msp430xG46x.h>

void main(void)
{
  WDTCTL = WDTPW + WDTHOLD;                 // Stop watchdog timer
  FLL_CTL0 |= DCOPLUS + XCAP18PF;           // DCO+ set, freq = xtal x D x N+1
  SCFI0 |= FN_4;                            // x2 DCO freq, 8MHz nominal DCO
  SCFQCTL = 121;                            // (121+1) x 32768 x 2 = 7.99 MHz
  P1DIR = 0x22;                             // P1.1 & P1.5 to output direction
  P1SEL = 0x22;                             // P1.1 & P1.5 to output MCLK & ACLK

  while(1);                                 // Loop in place
}
```

Demo #3 (XT2)

```
//******************************************************************************
//   MSP430xG46x Demo - FLL+, MCLK Configured to Operate from XT2 HF XTAL
//   Description: Proper selection of an external HF XTAL for MCLK is
//   demonstrated using HF XT2 OSC.  OFIFG is polled until the HF XTAL
//   is stable - only then is MCLK sourced by XT2.  MCLK is buffered on P1.1.
//                MSP430xG46x
//             -----------------
//         /|\|              XIN|-
//          | |                 |
//          --|RST          XOUT|-
//            |                 |
//            |            XT2IN|-
//            |                 | HF XTAL (455kHz - 8MHz)
//            |           XT2OUT|-
//            |                 |
//            |        P1.1/MCLK|-->MCLK = HF XTAL
//******************************************************************************
```

Demo #3 (XT2) cont'd

```c
#include  <msp430xG46x.h>

void main(void) {
  volatile unsigned int i;

  WDTCTL = WDTPW+WDTHOLD;     // Stop WDT
  // Disable LFXT1 xtal osc & FLL loop
  _BIS_SR(OSCOFF + SCG0 + GIE);
  // Activate XT2 high freq xtal
  FLL_CTL1 &= ~XT2OFF;
  // Wait for xtal to stabilize
  do
  {
    IFG1 &= ~OFIFG;           // Clear OSCFault flag
    for (i = 5; i > 0; i--);  // Time to set flag
   }
  // OSCFault flag still set?
  while ((IFG1 & OFIFG));
  FLL_CTL1 |= SELM1;    // MCLK = XT2

  P1DIR |= 0x002;     // P1.1 output direction
  P1SEL |= 0x002;     // P1.1 option select

  while(1);
}
```